

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: NAKAGAWA et al.
Serial No.: Rule 53(b) of 10/028,425
Filed: August 13, 2003
For: TERMINAL APPARATUS
Art Unit: Unassigned (2185 previously in parent application)
Examiner: Unassigned (C. Cao previously in parent application)

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §1.97 & §1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 13, 2003

Sir:

This Information Disclosure Statement is being filed in accordance with 37 C.F.R. §1.97 along with a Form PTO-1449. This Information Disclosure Statement is being filed simultaneously with the filing of this application.

This application claims priority under 35 U.S.C. §120 from U.S. Application No. 10/028,425 filed December 28, 2001, as well as U.S. Application No. 09/051,286 filed April 9, 1998. Thus, in accordance with 37 C.F.R. §1.98(d), copies of the references cited or submitted in the parent applications do not need to be filed by the applicant.

English language Abstracts were previously provided for each of JP-A-5-1228280, JP-A-4-219045, JP-A-4-167168 and JP-A-2-297594. Those four

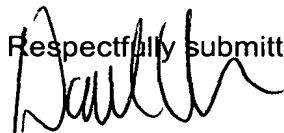
references as well as JP-U-3-080689 were also cited in a corresponding PCT Search Report.

Additionally, an English language Abstract of JP-A-9-22379 was also previously submitted.

It is respectfully requested that this Information Disclosure Statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (referencing Case No. 500.36179CC2) and please credit any excess fees to such deposit account.

Respectfully submitted,



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Attachments:
Form PTO-1449

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FORM PTO-1449 U.S. Department of Commerce
(Rev. 4/92) Patent and Trademark Office

ATTY. DOCKET NO.
500.36179CC2

SERIAL NO.
Rule 53(b) of 10/028,425

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

APPLICANT
NAKAGAWA et al.

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August 13, 2003

GROUP
Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4 7 7 9 1 9 2	10/88	TORII et al.			
	5 2 0 3 0 0 3	4/93	DONNER			
	6 2 3 0 2 5 5	5/01	ASGHAR et al.			
	5 2 9 3 5 8 6	3/94	YAMAZAKI et al.			
	5 3 1 5 7 0 0	5/94	JOHNSTON et al.			
	5 7 9 4 0 6 7	8/98	KADOWAKI			
	6 3 5 3 8 6 3	3/02	NAKAGAWA et al.			
	5 3 1 1 4 5 8	5/94	COVEY			
	5 5 1 9 8 7 9	5/96	CARMON			
	5 4 9 1 8 2 8	2/96	AFEK			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO
5 1 2 8 2 8 0	5/93	JP			
4 2 1 9 0 4 5	8/92	JP			
4 1 6 7 1 6 8	6/92	JP			
3 0 8 0 6 8 9	8/91	JP			
2 2 9 7 5 9 4	12/90	JP			
6 0 2 0 4 0 2 9	10/85	JP			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

1	"DSP56116 Digital Signal Processor User User's Manual" issued by Motorola Inc., pp. 1-1 to 5-16, 1990.
2	Nikkei Electronics Vol. 463, December 26, 1998 (Nikkei BP Corp.), Osamu Kobayashi and other, "DSP which spreads its application scope on the full-scale debut of 32-bit floating points" pp. 133-146, Figs. 5, 12.
3	"Latest Information on GSM/Systems, Terminals and Services", Seminar materials, Japan Industrial Technological Center, May 18 and 19, 1965 and "Development Trend of GSM telephone Terminal Devices", pp. 118-130, Japan Phillips.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in confidence and not considered. Include copy of this form with next communication to applicant.

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	6 0 4 7 3 5 8	4/00	JACOBS			
	5 3 9 2 4 4 8	2/95	FRANKEL et al.			
	4 7 9 1 5 9 0	12/98	KU et al.			
	5 5 6 7 9 0 0	10/96	HIGASHI			
	5 5 9 2 6 7 7	1/97	INTRATER et al.			
	5 6 3 0 1 5 3	5/97	INTRATER et al.			
	5 7 6 8 6 1 3	6/98	ASGHAR			
	5 8 6 7 7 2 6	2/99	OHSUGA et al.			
	5 8 8 4 0 9 2	3/99	KIUCHI et al.			
	5 3 1 1 4 5 8	5/94	HAINES et al.			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLAS S	TRANSLATION
					YES NO
0 0 9 2 2 3 7 9	1/97	JP			
0 4 4 2 0 4 1	8/91	EP			
0 4 6 5 0 5 4	1/92	EP			
40 7 0 1 3 5 6 1	1/95	JP			
9 7 1 4 0 9 3	4/97	WO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

4	"Hitachi Single-Chip RISC Microcomputers SH7032, SH7034 Hardware Manual", third edition, March 1964, issued by Hitachi, Ltd.
5	"A diversified application study for memory IC" Interface No. 123, August 1987 (CQ Publishing).
6	"Super RISC Engine SH7604 Hardware Manual", First Edition, September 1994, issued by Hitachi, Ltd.

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